Results **1** - **20** of about **1,230**. (**0.11** sec)

Dual channel FIFO circuit with a **single ported SRAM**
MH Kim, DW Shin - US Patent 5,745,731, 1998 - Google Patents
5,745,731 the maximum transfer of SCSI-IT, 10 MB/sec. In general, when the I/O commands of the SCSI side are executed, the FIFO 1 has data which are shorter than those to be transferred. Accordingly, when the FIFO 1 executes the SCSI commands, it must performs **...**
Cited by 6 - Related articles

Building and using a highly parallel programmable logic array
M Gokhale, W Holmes, A Kopser, S Lucas, R ... - Computer, 1991 - ieeexplore.ieee.org
... 82 COMPUTER Page 3. design. That left 32 stages, each with an FPGA and an **SRAM** chip. At that time, the biggest and fastest memories were **single- ported** 128Kx 8,50-nanosecond SRAMs. Thus, we were faced with choosing **...**
Cited by 251 - Related articles - All 3 versions

Power efficient processor architecture and the Cell processor psu.edu [PDF]
HP Hofstee - ieeexplore.ieee.org
... As an example, a second load-store port on a cache tends to double its size (a two-ported **SRAM** cell is often more than twice as big as a **single-ported** cell), and introduces the need to add logic to maintain the program order between loads and stores. **...**
Cited by 271 - Related articles - All 30 versions

Tradeoffs in two-level on-chip caching 202.38.79.74 [PDF]
NP Jouppi, SJE Wilton - Proceedings the 21st Annual ..., 1994 - ieeexplore.ieee.org
... This results in faster access times but a larger ratio of peripheral to **RAM** core cell area. In most of this paper, we will assume first-level **RAM** cells are 6-transistor **single-ported** cells allowing one read or write per cycle. Section 6, however, will consider larger multiported cells. **...**
Cited by 118 - Related articles - BL Direct - All 11 versions

A platform based bus-interleaved architecture for de-blocking filter in H. 264/MPEG-4 AVC psu.edu [PDF]
SC Chang, WH Peng, SH Wang, T ... - IEEE Transactions on ..., 2005 - ieeexplore.ieee.org
... 2. **Single-ported SRAM** A **single-ported SRAM** is used as a local memory for buffering the horizontally filtered and transposed MB. **...** This constraint is posed by the fact that **single-ported SRAM** cannot simultaneously perform writing and reading. **...**
Cited by 31 - Related articles - All 14 versions

Designing the TFP microprocessor
PYT Hsu - IEEE Micro, 1994 - ieeexplore.ieee.org
... Speed was a problem with tag comparisons for those schemes that are associative. Accordingly, we chose a simple, direct-mapped, one-bit prediction scheme that can be implemented entirely with a **single-ported RAM**. This **...**
Cited by 66 - Related articles - All 2 versions

Implementing signatures for transactional memory psu.edu [PDF]
D Sanchez, L Yen, MD Hill, K ... - 40th Annual IEEE/ACM ..., 2007 - ieeexplore.ieee.org
... To im- plement k hash function signatures, we should use SRAMs with k read and write ports (we could still use a **single- ported SRAM** and perform the reads or writes over multiple cycles, but that would complicate the control logic and in- crease the delay). **...**
Cited by 41 - Related articles - All 7 versions

Multi-ported memory architecture using **single-ported RAM**
M Miller, J Mick, J Smith, M Baumann, C ... - US Patent 6,212,607, 2001 - Google Patents
US006212607B1 (12) United States Patent Miller et al. (io) Patent No.: US 6,212,607 Bl (45) Date of Patent: Apr. 3,2001 (54) MULTI-PORTED MEMORY ARCHITECTURE USING **SINGLE-PORTED RAM** (75) Inventors: Michael Miller, Saratoga; John Mick, San Jose; **...**
Cited by 5 - Related articles

Network adapter having **single ported** memory which is accessible by network and peripheral bus on a time division multiplexed (TDM) basis
A Szczepanek - US Patent 5,832,216, 1998 - Google Patents
... other clock cycles. 4. An adapter according to claim 1, wherein the **single ported** memory comprises a **RAM**. 5. An adapter according to claim 1, wherein the **single ported** memory comprises an **SRAM**. 6. An adapter according **...**
Cited by 4 - Related articles

A streaming processing unit for a CELL processor
B Flachs, S Asano, SH Dhong, P ... - ... Solid-State Circuits ..., 2005 - ieeexplore.ieee.org
... local store (LS). Loads, stores and instruction fetch complete without exception, greatly simplifying the core design. The LS is a fully pipelined, **single-ported**, 256kb **SRAM** [3] that supports quadword (16B) or line (128B) access. **...**
Cited by 119 - Related articles

Interleaved cache for multiple accesses per clock cycle in a microprocessor
DB Alpert, MR Choudhury, JD Mills - US Patent 5,559,986, 1996 - Google Patents
... No. 4,823,314. The dual-ported memory cell is often used to accommodate multiple data references to a memory. How- ever, the dual-ported **RAM** cell requires two more transistors than a six transistor **single-ported SRAM** cell, two pairs of bit lines and two word lines. **...**

Cited by 24 - Related articles

Cache test sequence for **single-ported** row repair CAM
BW Hughes, WK Howlett - US Patent App. 09/792,476, 2001 - Google Patents
... 29, 2002 CACHE TEST SEQUENCE FOR **SINGLE-PORTED** ROW REPAIR CAM RELATED APPLICATIONS [0001] The present invention relates to commonly ... This memory is typically Static Random Access Memory (**SRAM**) or Dynamic Ran- dom Access Memory (DRAM). ...
Cited by 9 - Related articles - All 2 versions

[CITATION] SPACE 2 as a Re configurable Stream Processor
BK Gunther - Proceedings of PART'97, the 4th Australasian ..., 1993 - Springer
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[PS] Design of the R8000 Microprocessor unc.edu [PS]
PYT Hsu - IEEE Micro, 1994 - metalab.unc.edu
... Speed was a problem with tag comparisons for those schemes that are associative. Accordingly we chose a simple direct-mapped, one-bit prediction scheme which can be implemented entirely with a **single- ported RAM**. This ...
Cited by 29 - Related articles - View as HTML - All 16 versions

[PDF] Intel network processor targets routers udel.edu [PDF]
TR Halfhill - Microprocessor Report, 1999 - capsl.udel.edu
... There are 64 **SRAM** transfer registers and 64 SDRAM transfer registers. ... The banking scheme allows read/write instructions to retrieve and store results without the delays normally associated with **single- ported** register files, and without the complexity of multiple read and write ...
Cited by 32 - Related articles - View as HTML

Memory access optimization and **RAM** inference for pipeline vectorization markus-weinhardt.de [PDF]
M Weinhardt, W Luk - Field Programmable Logic and Applications, 1999 - Springer
... Though **RAM** inference can provide big speedups, it also uses many FPGA resources, especially if the candidate loops are long and consequently large RAMs ... je[1:m] pk j × xj,i ≤ maxp if Bi is dual-ported, that is accommodates twice as many accesses as **single-ported** memory. ...
Cited by 13 - Related articles - BL Direct - All 6 versions

[PDF] An eight-issue tree-VLIW processor for dynamic binary translation psu.edu [PDF]
K Ebcioglu, J Fritts, S Kosonocky, M Gschwind, ... - Proc. of the 1998 ..., 1998 - Citeseer
... The D1 cache is direct mapped and has 32 byte lines. The implementation for multiple ports uses **single-ported SRAM** arrays organized into 8 banks. Data is interleaved on a 32 byte line basis, with lines 0,8,16,... in bank 0, lines 1,9,17,... in bank 1 and so on. ...
Cited by 32 - Related articles - View as HTML - All 16 versions

An Industrial/Academic Configurable System-on-Chip Project (CSoC): Coarse-Grain XXP-/Leon-Based Architecture Integration
J Becker, A Thomas, M Vorbach, V ... - Proceedings of the ..., 2003 - portal.acm.org
... scenarios. In this way the XPP architecture is able to handle the data from a **RAM**-module or gets a stream from another master on the CSoC. The ... banks. The AHB-bridge for CM will be a **single ported** AHB- slave-bridge. The ...
Cited by 25 - Related articles - All 5 versions

A low-power self-timed Viterbi decoder man.ac.uk [PDF]
PA Riocreux, LEM Brackenbury, M Cumpstey, SB ... - async, 2001 - computer.org
... The reference design uses four **single-ported** 64-bit by 128 word SRAMs while the other synchronous designs use one, dual-ported 64-bit by 128 word, one 6-bit by 128 word **SRAM** and two small **single-ported** SRAMS. Our ...
Cited by 23 - Related articles - All 10 versions

Embedded static random access memory for field programmable gate array
WC Plants, J Joseph, AG Bell - US Patent 6,430,088, 2002 - Google Patents
... They include a column and/or multiple columns on their larger parts of embedded array blocks which are size matched to their logic array blocks. The embedded array blocks contain 2K bits of **single ported SRAM** configurable as 256x8, 512x4, 1024x2, or 2048x1. ...
Cited by 17 - Related articles - All 4 versions

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